



SOLDERABILITY OR SOLDERING ABILITY? THAT IS THE QUESTION:

While the environmental reasons for eliminating lead from solder are laudable, the switch has put electronics manufacturers on the back foot when it comes to determining the reliability of their products. Tried-and-trusted test methods – satisfactory for qualitative assessment of tin/lead joints – no longer apply, and new techniques must be put in place. IPC and IEC member Graham Naisbitt explains

Removing lead from electronics may be a good idea, but the transition to lead-free solder does dramatically alter the electronics assembly procedure, particularly for high-reliability products. Tin/lead solder joints have been comprehensively characterised over many decades, and manufacturers of products for safety-critical or life-dependent applications are able to reassure end users of their reliability.

This is not the case for lead-free alternatives. Although staff at standards bodies such as the Association Connecting Electronics Industries (IPC) and the International Electrotechnical Commission (IEC) have devoted many man-months to characterising solder joints formed using their recommended lead-free alloys, and proposing test regimes to ensure their reliability (see sidebar “Eliminating lead from electronics”), there is much more to do.

In addition, high-reliability products such as avionics systems or utility meters can have a life expectancy of up to 25 years. This means they are very likely to be subject to repair during their operational life. Rework procedures using tin/lead solder are proven and reliable, while questions inevitably remain about those formed from lead-free alloys.

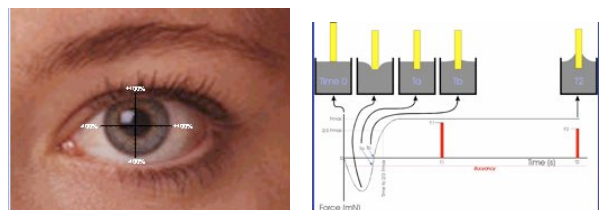
The task of fully characterising lead-free solder joints becomes doubly important when one considers that consumers might not feel so comfortable about moving quickly to substitutes if they realised there could be lingering doubts about lead-free reliability; especially if their lives depend on lead-free electronics such as being a

passenger on a commercial aircraft or in a vehicle equipped with an airbag.

Fortunately, manufacturers of high-reliability products have always taken a responsible approach towards ensuring the integrity of their products. Reliability is underwritten by a number of attributes, including good design, high quality components, and PCBs that are able to withstand shock, vibration and thermal excursions. Nonetheless, solder joints have always been considered a weak link and the introduction of lead-free solder has done nothing to mitigate the risk.

To lower to probability of failure, manufacturers routinely test component and PCB pad solderability. Without good solderability - a measure of how well molten solder wets component joints and PCB pads indicating the robustness of the surface finish - the likelihood of forming a reliable solder joint is dramatically diminished. Joints exhibiting poor solderability may still form a solder joint and even pass final electrical test; but the likelihood of failure due to stress, heat or vibration is high – unacceptable in a life-or-death application.

But the change to lead-free soldering – with its narrower process window - has exposed deficiencies in traditional test methods used to establish solderability such as “dip-and-look”. In this test a representative component is dipped in molten solder and the height the meniscus climbs is observed to gauge solderability.



Extensive testing by the IPC and IEC with many alloys, fluxes and components has revealed that dip-and-look lacks the “Gauge Repeatability & Reproducibility” (Gauge R&R) demanded to ensure the solder joints formed with a relatively uncharacterised material such as lead-free solder are as reliable as their tin/lead equivalents.

In this article I’ll explain why ensuring acceptable solderability is important for high reliability electronics, and why the transition to lead-free alloys has thrown the old



test methods into doubt. I'll also take a look at a solderability measurement that does satisfy the Gauge R&R criteria recommended by the IPC and IEC and explain how the tests are performed.

The importance of solderability testing

Component manufacturers and PCB makers prepare their devices for soldering by applying one of several surface finishes to the device termination's and pads on the board. Examples of surface finishes are organic solderability preservatives (OSPs), immersion tin and immersion silver, electrolytic and electroless nickel/gold, and fused or hot air-levelled solder.

These surface finishes – for which no standards yet exist - are designed to both protect the termination's and pads prior to assembly, and then provide a surface that encourages wetting by the solder during the reflow or wave solder operation. While each surface finish has its merits, it is generally agreed that solder is the best finish when fusing to solder paste or itself.

Unfortunately, all surface finishes are subject to a degree of degradation. And that degradation is influenced by factors such as storage conditions and times. The UK's world renowned National Physical Laboratory (NPL), for example, has conducted extensive studies into "solderability ageing" and the mechanisms of degradation.

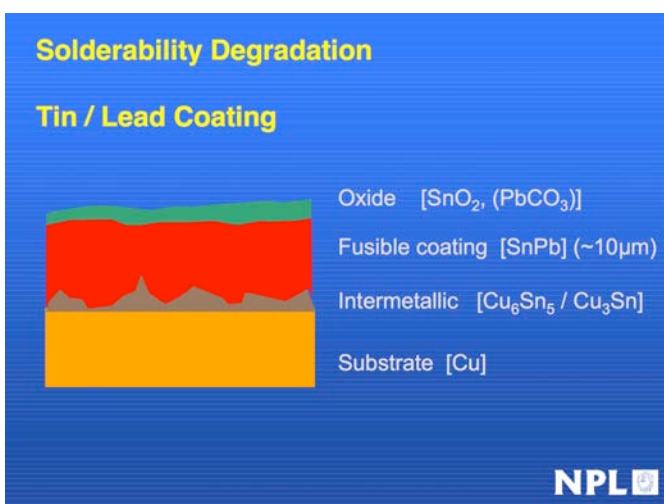


Figure 1 - Courtesy of The NPL

Figure 1 from the NPL shows that a tin/lead coating comprises three layers sitting on the pad substrate. The top layer is an oxide that must be stripped away by the flux

prior to soldering otherwise wetting will be poor. The second layer is the fusible coating that encourages good wetting, and the final layer is an intermetallic created by an interaction between the copper in the substrate and the tin from the fusible coating. This layer does not wet.

In simple terms the mechanism that causes solderability degradation is down to thickening of the oxide and intermetallic layer. The rate of growth is influenced by storage factors such as humidity, temperature and time. Figure 2 demonstrates the effect of oxide and intermetallic growth over time on solderability. It can be seen that solderability decreases as a function of ageing. Stages I and II represent areas where soldering is possible, stage III represent soldering failure. Note the diagrams at the bottom showing the geometry of the solder fillet at the various stages.

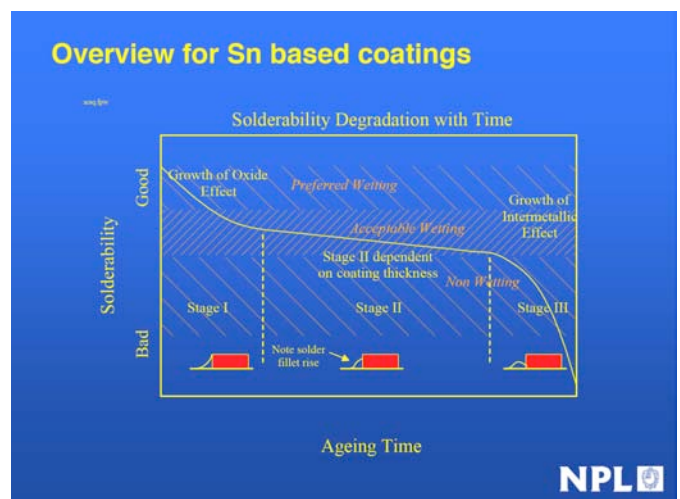


Figure 2 - Courtesy of The NPL

Measure solderability, not soldering ability

Experienced manufacturing engineers are well aware of this failure mechanism, and routinely take steps to determine if their components and PCBs are still satisfactory prior to assembly. However, the methods they use to test whether solder joints will last the life of the product have been called into question by the migration to lead-free alloys and the IPC's and IEC's comprehensive testing. To make matters worse, there is an industry-wide lack of understanding as to what attribute is actually being tested.

The problem is that manufacturers often fail to draw a clear distinction between solderability – how well molten solder wets – and soldering ability – a term used to describe how



well a specific combination of flux and solder work together to ensure a component is soldered to a PCB. They are not the same thing.

It's important to note that a device with "unacceptable" solderability (according to the standards) can often still be soldered with the "right" combination of flux and solder. For example, manufacturers can compensate for poor solderability by increasing flux volumes during production thus improving the soldering ability of the assembly. But that's no longer an option when using lead-free alloys for two reasons: The much narrower process window for lead-free soldering is less forgiving of process changes during production (increasing the likelihood of forming a suspect joint) and because additional flux has a detrimental effect on board cleanliness (particularly one assembled using a no-clean process).

The graphs in figures 3(a) and 3(b) illustrate this latter point (courtesy: NPL). These show the drop in surface insulation resistance (SIR) resistance as the flux volume increases on a standard test coupon. The drop in the curves corresponds to electrically conductive areas of the board formed by the flux residues after evaporation of volatile components. These conductive areas could contribute to medium- and long-term board failures.

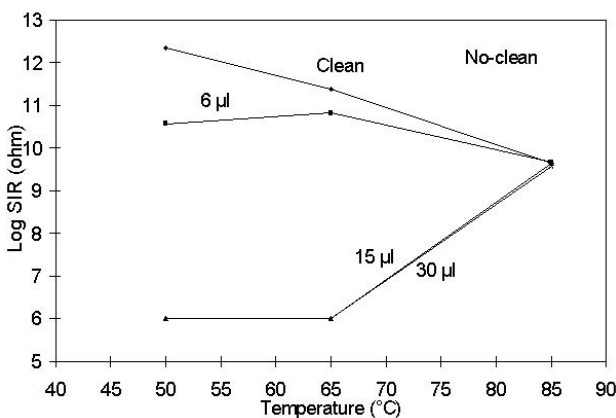


Figure 3(a) - showing flux volatilisation at temperature

The IPC's and IEC's analyses have established that the most important criterion for ensuring that lead-free soldering produces high integrity interconnections - while maintaining tight process control and limiting potentially failure-inducing contamination - is "acceptable" solderability.

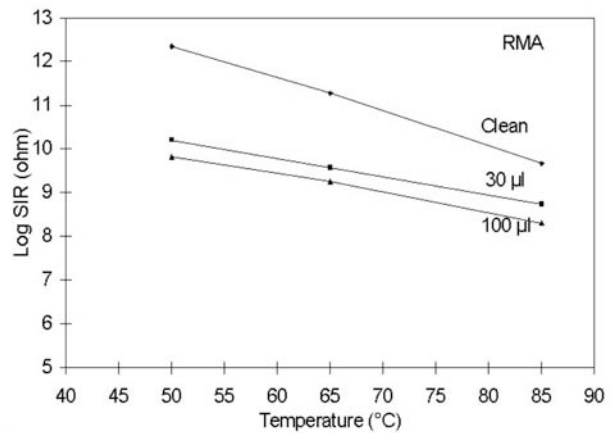


Figure 3(b) - showing the volume effect on SIR values

"Solderability evaluations are made to verify that the solderability of component leads and termination's meets the established requirements and to determine that storage has had no adverse effect on the ability to solder the component to the board," notes the IPC J-STD-002C & 003B documents.

And, as David Hillman, Chairman of IPC-J-STD 002 and 003 puts it: "The JSTD-002/003 solderability test standard's purpose is to test the robustness of a finish for wettability. Too many people attempt to use and/or believe that the standards are designed to mimic production conditions, they are not. This would be 'soldering ability' not 'solderability'.

"Although the IPC committee has attempted to have the standards reflect soldering ability concerns, it is not possible or practical in terms of testing methodology to mimic production. There are so many flux/process combination that the standards would cease to be of value; they would be huge and contain a multitude of variations.

"The test parameters contained in the standards are designed to have some safety margin in terms of demonstrating the solderability of a surface - a test which gives either a false positive or false negative result is not of value to the industry."

In other words, testing a component using a manufacturers regular component/flux/solder combination to ascertain the solderability of a surface finish doesn't adhere to any standard and isn't likely to provide the kind of repeatable or reproducible result demanded by an unforgiving lead-free soldering process.



Although soldering ability testing does have a place for qualitatively checking if your process flux and solder alloy are working well, it's not scientifically controllable enough to form the basis of a benchmark standard for solderability testing.

Choosing the correct test method

So how do you ensure you are measuring solderability rather than soldering ability for your lead-free assembly process?

To answer this question, the IPC committee agreed to undertake a "round-robin" test program to study the characteristics of lead-free alloys and fluxes. The round-robin tests looked at:

Alloy

Surface finish

Temperature

Flux

Gauge R&R.

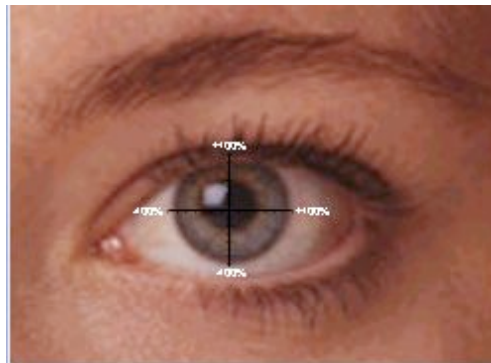
The standards, which are due to be published imminently, will also formally clarify the difference between solderability and soldering ability. The standards will define a process for solderability testing that precisely specifies the test equipment, how the test should be conducted, and the materials to be used to ensure good Gauge R&R.

For example, for a precision solderability test it is recommended that the test flux is carefully maintained and kept free of contamination during measurement (see IPC J-STD-002C sections 3.2.2.1 and 3.5.2). This includes either covering the flux when not in use and discarding it after eight hours or maintaining it to a specific gravity of 0.843 ± 0.005 at 25 ± 2 C (77 ± 3.6 F) and discarding it after one week of use.

Furthermore, the solder in the solder bath used for solderability testing should also be chemically or spectrographically analysed or replaced each 30 operating days according to strict standard-defined contamination limits. This includes the composition of the lead-free solder (including maximum contamination levels) being maintained during testing with the silver and copper element levels adjusted for alloy requirements.

It's easy to see that this isn't a regime that can be maintained using flux and solder from day-to-day production.

But what of the test methodology itself? Is the decades-old dip-and-look test method formalised in standards such as J-STD-002 and 003 an acceptable solution?



In this test (which is well defined), technicians dip representative component samples into a molten solder bath and observe how far the meniscus climbs. With experience, this provides a qualitative measure of solder wetting and hence solderability. The method is also quick, easy and cheap to implement.

The major problem with dip-and-look, however, is that as a test method it exhibits poor Gauge R&R. In other words, even if the materials used for the test are strictly controlled (as required by the new standards), two people conducting the test at different times are likely to interpret the results differently. What kind of basis is there for quality control of lead-free assembly if one person says the component and/or bare board is fine but another says it's not, depending on the time and place of the test?

"Users who believe that the dip-and-look methodology has a respectable Gauge R&R would be in for an extreme shock," says the IPC. Backing up these comments the IPC also adds: "The IPC committees have voted that no new solderability test methods will be introduced into the standards without a demonstrated, industry acceptable Gauge R&R value."

While this recommendation is not presently included in the IEC Standards, the committee have agreed to commence a further revision within 2 years, instead of the normal 5 years, and solderability testing with acceptable Gauge R&R will be included at that time. That could sound the death knell for dip-and-look testing.



Force measurement recommended

So what's the alternative? According to the IEC: "[We recommend] wetting balance force measurement and globule testing and we are attempting to harmonise standards documents, to provide acceptable Gauge R&R to its defined methodology."

Solderability measurements using a wetting balance measures force to an extremely high level of accuracy (to a resolution of milli-Newtons). Some electronics-based instruments (Gen3 Systems MUST) even measure to levels of better than $1\mu\text{N}/\text{Bit}$. Although the type of wetting balance used for plated through-hole (PTH) and surface mount (SM) components differs, both are based on the same physical principles. Namely: if a metallic body is dipped into molten solder, the weight and speed with which the solder meniscus climbs upwards on the body's immersed surface indicates how well the solder wets it and thus its solderability. The greater the solderability, the higher the meniscus will climb and that can be measured as a change in the vertical force action on the suspended specimen. (See Figure 4)



Time for change

The introduction of lead-free has disrupted a process – assembly using tin/lead solder – that has been characterised over many decades. The knock-on effect is that the IPC and IEC have determined – after extensive examination involving over 30,000 tests – that traditional test methods and process corrections are no longer sufficient to determine the reliability of lead-free joints.

New methods and clarifications of the difference between solderability and soldering ability are due from the organisations before the end of this year. These are likely to conclude that solderability testing is essential for manufacturers wanting to underwrite the integrity of their high-reliability products.

Moreover, the standards will conclude that solderability testing should be based on wetting balance force rather than dip-and-look. This former method will ensure a quantitative measure of the robustness of a given surface finish under test, with acceptable Gauge R&R while removing any scope for opinion or "manual" judgement calls that typically occur with dip-and-look.

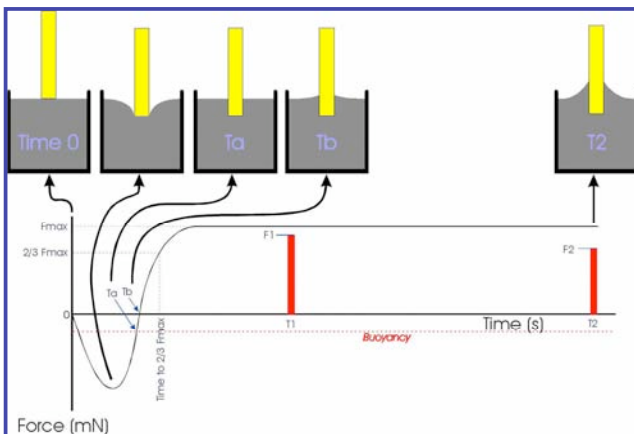
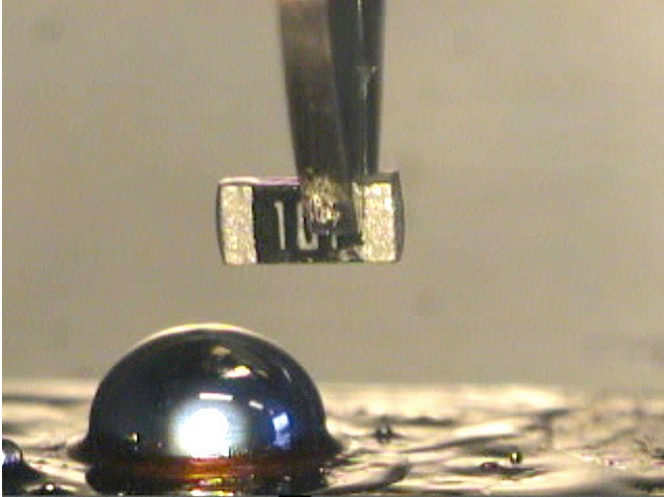


Figure 4 - Force Measurement explained

For certain TH components and circuit board coupons, the specimen device is immersed in a bath of molten solder and the forces of buoyancy and surface tension action upon it are measured. For smaller SMDs, a higher resolution method is required: the microwetting balance procedure (figure 5) that employs a solder globule. Here the solder bath is replaced by a globule block of 4, 3.2, 2 or 1-mm size employing 200, 100, 25 or 5-mg pellets of solder alloy (depending on specimen size) allowing the individual leads of a multi-leaded component to be tested.



ABOUT THE AUTHOR:

Graham Naisbitt is Managing Director of Gen3 Systems Limited (founded on Concoat Systems) and is a member of the IEC's TC91 WG3, the working group that formulates test standards for the assembly industry. Naisbitt is also Leader of Solderability Testing Standard IEC 60068-2-69, Co-leader of Solderability Testing Standard IEC 60068-2-54, and Member of IPC-J-STD 002 and IPC-J-STD 003. More information on solderability testing can be found on Gen3 Systems' web-site at www.gen3systems.com

Eliminating lead from electronics

The electronics industry has grown up with tin/lead solder. The IPC and IEC define these alloys as Sn60Pb40A, Sn63Pb37A or Sn62Pb36Ag02B. Over four decades the long-term performance of tin/lead alloys has been intensely studied. The standards bodies have issued comprehensive documentation, standards and test methodologies that allow manufacturers to ascertain the reliability of their electronics assemblies.

Lead is now banned from electronics assemblies and intended for sale in the EU. Legislation of a similar nature is likely to be introduced in Japan, California and China. Both IPC and IEC committees are working hard to try and ensure that revisions to the existing standards are published as quickly as possible, but neither group will have published documents until late 2006. However, both organisations are recommending high tin alloys as the best replacements for

tin/lead.

Specifically, the IPC states: "The solder composition shall be tin (Sn)96.5 silver (Ag)3.0 copper (Cu)0.5 (SAC305) as defined by J-STD-006". The IPC does allow other lead-free solder alloys if agreed between user and vendor.

The IEC states: "The preferred alloy composition should be either Sn96.5Ag3.0Cu0.5 or Sn99.3Cu0.7. An alloy consisting of 3-4% Ag and 0.5-1% Cu with the remainder made up of Sn may also be used instead of Sn96.5Ag3.0Cu0.5. A solder alloys comprising 0.45-0.9% Cu with the remainder made up of Sn may be used instead of Sn99.3Cu0.7."

Despite the work done so far, the fact remains that high tin alloys have not been as well characterised as traditional tin/lead solders. While the IPC and IEC have been rapidly assimilating data on the long-term performance of lead-free alloys it will be some time before comprehensive information is available. Accordingly, both organisations are defining thorough testing regimes – with acceptable Gauge R & R - for manufacturers whose products will be used in safety critical applications.

